

CLAIMS

What is claimed is:

1. An Ahuja compensation circuit, comprising:

first and second transistors, wherein a second terminal of said first transistor communicates with a control terminal of said second transistor;

first, second, and third capacitances, wherein a first end of said first capacitance communicates with said second terminal of said first transistor, a first end of said second capacitance communicates with a first terminal of said second transistor, and a second end of said third capacitance communicates with said first terminal of said second transistor, and

a high swing cascode biasing circuit that communicates with said second terminal of said first transistor and a first end of said third capacitance and that includes:

a current biasing circuit that generates a cascode bias and a main bias;

a frequency boosting circuit that receives said cascode bias and said main bias; and

a current mirror circuit that receives said main bias.

2. The Ahuja compensation circuit of Claim 1 wherein feedback is used to increase a transconductance of said high swing cascode biasing circuit.

3. The Ahuja compensation circuit of Claim 1 wherein said current mirror circuit comprises:

third and fourth transistors, wherein a second terminal of said third transistor communicates with a first terminal of said fourth transistor, a first terminal of said third transistor communicates with said control terminal of said second transistor, and said second terminal of said third transistor communicates with said first end of said third capacitance.

4. The Ahuja compensation circuit of Claim 3 wherein said current biasing circuit comprises:

fifth, sixth, seventh, and eighth transistors each having a first terminal, a second terminal, and a control terminal, wherein said second terminals of said fifth and seventh transistors communicate with said first terminals of said sixth and eighth transistors, respectively, said control terminals of said fifth and sixth transistors communicate, said first terminal of said fifth transistor communicates with said control terminal of said seventh transistor, and said control terminal of said eighth transistor communicates with said first terminal of said seventh transistor.

5. The Ahuja compensation circuit of Claim 4 wherein control terminals of said third and fourth transistors communicate with said control terminals of said seventh and eighth transistors, respectively.

6. The Ahuja compensation circuit of Claim 4 wherein said current biasing circuit further comprises a fourth capacitance having a first end that communicates with said second terminal of said fifth transistor.

7. The Ahuja compensation circuit of Claim 4 wherein said frequency boosting circuit comprises:

a resistance having a first end that communicates with said first terminal of said fifth transistor and a second end that communicates with said control terminal of said fifth transistor; and

a fourth capacitance having a first end that communicates with said second end of said resistance and a second end that communicates with said second terminal of said third transistor.

8. The Ahuja compensation circuit of Claim 4 wherein said first, second, third, fourth, fifth, sixth, seventh, and eighth transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

9. The Ahuja compensation circuit of Claim 8 wherein said resistance is one of a standard fixed-value resistor, a nonlinear resistor, and a metal-oxide semiconductor (MOS) resistor.

10. The Ahuja compensation circuit of Claim 4 wherein said first terminals of said fifth and seventh transistors communicate with first and second current sources, respectively.

11. The Ahuja compensation circuit of Claim 1 wherein an input voltage of said Ahuja compensation circuit is applied to a control terminal of said first transistor and wherein an output voltage of said Ahuja compensation circuit is referenced from said first terminal of said second transistor.

12. The Ahuja compensation circuit of Claim 1 wherein said first terminal of said second transistor communicates with a current source.

13. A feedback loop in an Ahuja compensation circuit, comprising:
- a first transistor;
 - a first capacitance having a first end that communicates with a first terminal of said first transistor; and
 - a high swing cascode biasing circuit that communicates with a second end of said first capacitance and a control terminal of said first transistor and that includes:
 - a current biasing circuit that generates a cascode bias and a main bias;
 - a frequency boosting circuit that receives said cascode bias and said main bias; and
 - a current mirror circuit that receives said main bias.
14. The feedback loop of Claim 13 wherein said current mirror circuit comprises:
- second and third transistors, wherein a second terminal of said second transistor communicates with a first terminal of said third transistor, a first terminal of said second transistor communicates with said control terminal of said first transistor, and said second terminal of said second transistor communicates with said first end of said first capacitance.

15. The feedback loop of Claim 14 wherein said current biasing circuit comprises:

fourth, fifth, sixth, and seventh transistors each having a first terminal, a second terminal, and a control terminal, wherein said second terminals of said fourth and sixth transistors communicate with said first terminals of said fifth and seventh transistors, respectively, said control terminal of said fourth transistor communicates with said control terminal of said fifth transistor, said first terminal of said fourth transistor communicates with said control terminal of said sixth transistor, and said control terminal of said seventh transistor communicates with said first terminal of said sixth transistor.

16. The feedback loop of Claim 15 wherein control terminals of said second and third transistors communicate with said control terminals of said sixth and seventh transistors, respectively.

17. The feedback loop of Claim 15 wherein said current biasing circuit further comprises a second capacitance having a first end that communicates with said second terminal of said fourth transistor.

18. The feedback loop of Claim 15 wherein said frequency boosting circuit comprises:

a resistance having a first end that communicates with said first terminal of said fourth transistor and a second end that communicates with said control terminal of said fourth transistor; and

a second capacitance having a first end that communicates with said second end of said resistance and a second end that communicates with said second terminal of said second transistor.

19. The feedback loop of Claim 15 wherein said first, second, third, fourth, fifth, sixth, and seventh transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

20. The feedback loop of Claim 18 wherein said resistance is one of a standard fixed-value resistor, a nonlinear resistor, and a metal-oxide semiconductor (MOS) resistor.

21. The feedback loop of Claim 15 wherein said first terminals of said fourth and sixth transistors communicate with first and second current sources, respectively.

22. A system comprising the feedback loop of Claim 13 and further comprising an Ahuja compensation circuit including said first transistor and a second transistor, wherein a second terminal of said second transistor communicates with said control terminal of said first transistor.

23. The system of Claim 22 wherein an input voltage of said system is applied to a control terminal of said second transistor and wherein an output voltage of said system is referenced from said first terminal of said first transistor.

24. The system of Claim 22 wherein said Ahuja compensation circuit comprises second and third capacitances, wherein a first end of said second capacitance communicates with said control terminal of said first transistor and wherein said first end of said third capacitance communicates with said first terminal of said first transistor.

25. The feedback loop of Claim 13 wherein said first terminal of said first transistor communicates with a first current source.

26. A feedback loop in an Ahuja compensation circuit, comprising:
- a first transistor;
 - first capacitance means for providing a first capacitance and having a first end that communicates with a first terminal of said first transistor; and
 - high swing cascode biasing means for communicating with a second end of said first capacitance means and a control terminal of said first transistor and that includes:
 - current biasing means for generating a cascode bias and a main bias;
 - frequency boosting means for receiving said cascode bias and said main bias and for boosting a frequency response of said high swing cascode biasing means; and
 - current mirror means for receiving said main bias.

27. The feedback loop of Claim 26 wherein said current mirror means comprises:
- second and third transistors, wherein a second terminal of said second transistor communicates with a first terminal of said third transistor, a first terminal of said second transistor communicates with said control terminal of said first transistor, and said second terminal of said second transistor communicates with said first end of said first capacitance means.

28. The feedback loop of Claim 27 wherein said current biasing circuit comprises:

fourth, fifth, sixth, and seventh transistors each having a first terminal, a second terminal, and a control terminal, wherein said second terminals of said fourth and sixth transistors communicate with said first terminals of said fifth and seventh transistors, respectively, said control terminal of said fourth transistor communicates with said control terminal of said fifth transistor, said first terminal of said fourth transistor communicates with said control terminal of said sixth transistor, and said control terminal of said seventh transistor communicates with said first terminal of said sixth transistor.

29. The feedback loop of Claim 28 wherein control terminals of said second and third transistors communicate with said control terminals of said sixth and seventh transistors, respectively.

30. The feedback loop of Claim 28 wherein said current biasing means further comprises second capacitance means having a first end that communicates with said second terminal of said fourth transistor.

31. The feedback loop of Claim 28 wherein said frequency boosting means comprises:

resistance means for providing resistance and having a first end that communicates with said first terminal of said fourth transistor and a second end that communicates with said control terminal of said fourth transistor; and

second capacitance means for providing a second capacitance and having a first end that communicates with said second end of said resistance means and a second end that communicates with said second terminal of said second transistor.

32. The feedback loop of Claim 28 wherein said first, second, third, fourth, fifth, sixth, and seventh transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

33. The feedback loop of Claim 31 wherein said resistance means is one of a standard fixed-value resistor, a nonlinear resistor, and a metal-oxide semiconductor (MOS) resistor.

34. The feedback loop of Claim 28 further comprising first and second current means for providing current, wherein said first terminals of said fourth and sixth transistors communicate with said first and second current means for providing current, respectively.

35. A system comprising the feedback loop of Claim 26 and further comprising an Ahuja compensation means for providing Ahuja compensation and including said first transistor and a second transistor, wherein a second terminal of said second transistor communicates with said control terminal of said first transistor.

36. The system of Claim 35 wherein an input voltage of said system is applied to a control terminal of said second transistor and wherein an output voltage of said system is referenced from said first terminal of said first transistor.

37. The system of Claim 35 wherein said Ahuja compensation means further comprises second and third capacitance means for providing capacitance, wherein a first end of said second capacitance means communicates with said control terminal of said first transistor and wherein said first end of said third capacitance means communicates with said first terminal of said first transistor.

38. The feedback loop of Claim 26 further comprising first current means for providing current wherein said first terminal of said first transistor communicates with said first current means.